Input Clocking Considerations on the HMC1520

Product Application Note

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1 Introduction

The HMCAD1520 operates from one clock input, which can be differential or single ended. The clock pins are AC-coupled internally; hence a wide common mode voltage range is accepted. Differential clock sources such as LVDS, LVPECL or differential sine wave can be utilized. LVDS/LVPECL clock signals must be appropriately terminated as close as possible to the ADC clock input pins.

For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. CMOS inputs are not recommended above 200MHz. For differential sine wave clock input the amplitude must be at least +/- 0.8 Vpp. No additional configuration is needed to set up the clock source format.

The HMCAD1520 only uses the rising edge of the input clock. Hence, clock duty cycles between 30% and 70% are acceptable. As in all high speed ADCs, the quality of the input clock is extremely important and it is of utmost importance to limit the clock jitter. Use precise and stable clock references or re-time using a low jitter master clock as the last operation before the signal is applied to the ADC clock input. At 100 MSPS sampling speed, 1ps of clock jitter will introduce a -64 dBc SNR signal component. Avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The sampling clocks for each of the four channels are generated from the clock input using a carefully matched clock buffer tree. Internal clock dividers are utilized to control the clock for each ADC during interleaving. The clock tree is controlled by the Mode of Operation (Tables 2 and 3).

2 Clock Division

The *clk_divide<1:0> register* allows the user to apply an input clock frequency higher than the sampling rate. The clock divider will divide the input clock frequency by a factor of 1, 2, 4, or 8 as per Table 1. By setting the *clk_divide<1:0>* value relative to the *high_speed_mode <2:0>* value (Table 3), the same input clock frequency can be used for all settings on number of channels.

For example, when increasing the number of channels from 1 to 4, the maximum sampling rate is reduced by a factor of 4. By letting *clk_divide<1:0>* follow the *high_speed_mode<2:0>* value, and change it from 1 to 4, the internal clock divider will provide the reduction of the sampling rate without changing the input clock frequency.

clk_divide<1:0>	Clock Divider Factor	Sampling rate (FS)
00 (default)	1	Input clock frequency / 1
01	2	Input clock frequency / 2
10	4	Input clock frequency / 4
11	8	Input clock frequency / 8

Table 1 Clock Divider Factor

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Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
precision_mode	Enable Quad Channel 14 bits precision mode.	Inactive													X				0x31
high_speed_mode <2:0>	Enable high speed mode, Single, Dual or Quad channel.	High speed mode – Quad Channel														X	X	X	
clk_divide<1:0>	Define clock divider factor: 1, 2, 4 or 8	Divide by 1							X	X									

Table 2 Modes of Operation (1)

precision _mode	high_speed_mode <2:0>			Mode of operation	Description
0	0	0	1	Single channel 12-bit high speed mode	Single channel by interleaving ADC1to ADC4
0	0	1	0	Dual channel 12-bit high speed mode	Dual channel where channel 1 is made by interleaving ADC1 and ADC2, channel 2 by interleaving ADC3 and ADC4
0	1	0	0	Quad channel 12-bit high speed mode	Quad channel where channel 1 corresponds to ADC1, channel2 to ADC2, channel3 to ADC3 and channel 4 to ADC4
1	0	0	0	Quad channel 14-bit precision mode	Quad channel where channel 1 corresponds to ADC1, channel2 to ADC2, channel3 to ADC3 and channel 4 to ADC4

Table 3 Modes of Operation (2)

3 Start-up

To optimize start up time, a register is provided where the start-up time in clock cycles can be set. Some internal circuitry have start-up times that are clock frequency independent. Default counter values are set to accommodate these start up times at the maximum clock frequency (sampling rate). This will lead to increased start up times at low clock frequencies. Setting the value of this register to the nearest higher clock frequency will reduce the count values of the internal counters, to better fit the actual start up time, such that the start-up time will be reduced (See Table 5). The start-up times from power down and sleep modes are changed by this register setting. If the clock divider is used (set to other than 1), the input clock frequency must be divided by the divider factor to find the correct clock frequency range (see Table 1)

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
startup_ctrl <2:0>	Controls start-up time	'000'														X	X	X	0x56

Table 4 Start-up Time Control

Precision mode					Quad channel – High speed			
startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]		startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]
100	80 - 125	1536	12.3 - 19.2		100	160 - 250	3072	12.3 – 19.2
000	50 - 80	992	12.4 - 19.8		000	100 - 160	1984	12.4 - 19.8
001	32,5 - 50	640	12.8 - 19.7		001	65 - 100	1280	12.8 - 19.7
010	20 - 32,5	420	12.9 - 21		010	40 - 65	840	12.9 - 21
011	15 - 20	260	13 - 17.3		011	30 - 40	520	13 - 17.3
other	Do not use	-	-		other	Do not use	-	-
Dual channel – High speed					Single channel – High speed			
startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]		startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]
100	320 - 500	6144	12.3 – 19.2		100	640 - 1000	12288	12.3 – 19.2
000	200 - 320	3968	12.4 - 19.8		000	400 - 640	7936	12.4 - 19.8
001	130 – 200	2560	12.8 - 19.7		001	260 - 400	5120	12.8 - 19.7
010	80 - 130	1680	12.9 - 21		010	160 - 260	3360	12.9 - 21
011	60 – 80	1040	13 - 17.3		011	120 - 160	2080	13 - 17.3
other	Do not use	-	-		other	Do not use	-	-

Table 5 Start-up Time Settings

4 Internal Clock Jitter

jitter_ctrl<7:0> allows the user to set a trade-off between power consumption and clock jitter. If all bits in the register is set low, the clock signal is stopped. The clock jitter depends on the number of bits set to '1' in the *jitter_ctrl<7:0>* register as per Table 7. Exactly which bits are set high does not affect the result.

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
jitter_ctrl <7:0>	Clock jitter adjustment	160 fsrms									X	X	X	X	X	X	X	X	0x30

Table 6 Jitter Control

Number of bits to '1' in jitter_ctrl<7:0>	Clock jitter performance Precision mode [fsrms]	Clock jitter performance High speed modes [fsrms]	Module current consumption [mA]
1	130	160	1
2	100	150	2
3	92	136	3
4	85	130	4
5	82	126	5
6	80	124	6
7	77	122	7
8	75	120	8
0	Clock stopped	Clock stopped	

Table 7 Jitter Performance

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